

REAL-SPACE STRAIN MAPPING OF SOI FEATURES USING MICROBEAM X-RAY DIFFRACTION

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The implementation of strain in microelectronic technology represents an important aspect of the enhancement in CMOS device performance. An understanding of the mechanical response of the Si channel regions and their environment is key to the prediction and design of device operation. Strain can be induced through residual stresses present in deposited layers or through the processing of structures with dissimilar thermal expansion behavior. Because of the complexity of the composite geometry associated with microelectronic circuitry, characterization of the Si strain at a submicron resolution is necessary to verify the predicted strain distributions. Synchrotron-based x-ray microbeam measurements were performed on silicon-on-insulator (SOI) features strained by adjacent shallow-trench-isolation (STI). The interaction region of the SOI strain was observed to extend at least 25 times the SOI film thickness from the STI edge. Regions of 65 nm thick SOI less than 3 μm wide exhibited an overlap in the strain fields due to the surrounding STI. Results will be also presented of the spatial distribution of strain in SOI induced by overlying silicon nitride structures.