

## READOUT ASICs FOR SILICON DRIFT DETECTORS

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Semiconductor Drift Detectors (SDD) have nowadays reached a leading position as detectors for X-ray spectroscopy due to their outstanding performances in terms of energy-resolution and high detection rate. These performances can nevertheless be exploited at the best only with specifically and carefully designed readout electronics. An ASIC (Application Specific Integrated Circuit) solution for the SDD may provide a more compact assembly of the detection module, especially when more channels are involved. We discuss here the critical aspects of the readout process and present the experimental results recently obtained with new ASIC circuits specifically designed for SDDs.

The SDD's performances are basically due to their very small output capacitance. The integration of the input JFET of the preamplifier directly on the detector maximizes the benefits of the low output capacitance. The readout electronics here presented has been designed for SDDs with integrated JFET.

The charge preamplifier operating in the pulse-reset regime is presently the most used solution thanks to its low noise performances achievable also at high counting rates. The noise associated to the anode discharge current can in fact be avoided. Moreover the gain stability is greatly improved by the feedback configuration. A four channel integrated CMOS version of the preamplifier has been realized and tested. With a droplet SDD an energy resolution of 126eV FWHM has been achieved with this preamplifier (Fig.1), equal to the one achievable with a hybrid preamplifier operating with the same detector sample.

Specifically for high counting rates measurements, we have developed an ASIC with charge preamplifier and a high-order fast shaping amplifier. It consists of a 9<sup>th</sup> order filter optimized to achieve good electronics noise together with a reduced pulse width to minimize the pile-up probability. The pulse width, here defined as the time duration of the pulse waveform within 1% of its maximum amplitude, has been defined to guarantee a dead time lower than 30% at 500.000 counts/s still keeping a good energy resolution. In Fig. 2, a photograph of the ASIC is shown, while in Fig.3 the measured waveform of the shaper together with the one of the preamplifier is reported. The spectrum of a Fe-55 source has been measured with a SDD droplet type of 10mm<sup>2</sup> active area and the integrated circuit. The energy resolution FWHM measured with a shaping time of 250ns, set not for optimum resolution but to provide high throughput, is still as good as 142eV FWHM.

Multi-channel ASICs, up to 25-channels parallel readout, designed for multi-channels applications will be also described, together with the performances achieved when used with multi-channels SDDs.

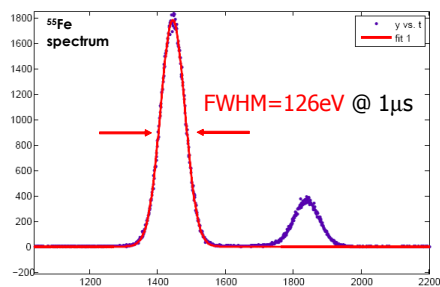


Fig. 1 – Energy spectrum of a Fe-55 source measured with a SDD of 10mm<sup>2</sup> and the preamplifier ASIC. The shaping time is 1μs.

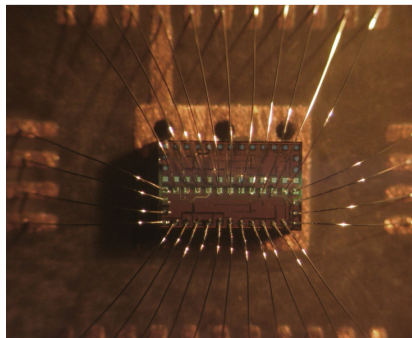


Fig. 2 – Photograph of the ASIC including charge preamplifier, fast shaper and peak stretcher.

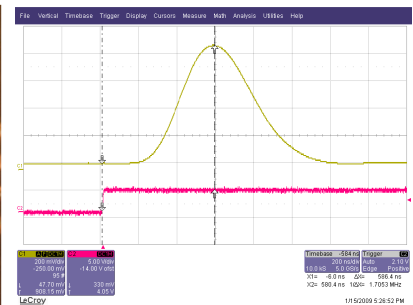


Fig. 3 – Output waveform of a 9 poles integrated shaping amplifier, together with the preamplifier waveform.