

UNDERSTANDING STRESS GRADIENTS IN MICROELECTRONIC METALLIZATION

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The manufacture of ultra-large scale integration technology involves many thermal excursions that can impose significant strain within the constituent metallization due to the mismatch in coefficients of thermal expansion between metallization and its environment. The resulting stress distributions can be large enough to induce voiding within Cu-based metallization, a key reliability issue that must be addressed. In particular, the interface between the Cu and overlying capping layers is a critical location associated with void formation. By combining conventional and glancing-incidence X-ray diffraction measurements, we can investigate depth-dependent stress distributions that develop in Cu films and patterned features. Results from in-situ annealing and as-deposited measurements will be presented showing that strain gradients are created in capped Cu structures, where an increased in-plane tensile stress is generated near the Cu / cap interface. The interplay between plasticity in the Cu and the constraint imposed by capping layers dictates the extent of the observed gradients. For example, Cu films possessing caps deposited in a temperature regime where the Cu experienced only elastic deformation did not exhibit depth-dependent stress distributions. The effects of cap composition and geometry of the low-k dielectric / metallization composite will be discussed. However, all capped Cu samples exposed to temperatures high enough to induce plastic behavior developed greater tensile stress at the Cu / cap interface than in the bulk Cu after cooling, representing a clear concern to the mitigation of metallization voiding.