VERDI-3: NEW IMPROVEMENTS IN MULTI-DETECTOR READOUT ASIC

A.Celani[1], R. Quaglia[2], C. Fiorini[2], T.Frizzi[1], O.Evrard[3], C. Cherukuri[3], B.Zakrzewski[4], J.Pavlick[4]

[1]XGLab s.r.l., Via Moretto da Brescia 23, I-20133, Milano, Italy, ph +390249660460, email info@xglab.it

[2]Politecnico di Milano, Dipartimento di Elettronica e Informazione, Piazza L. da Vinci, I-20133, Milano, Italy

[3]Canberra Semiconductors N.V., Olen, Belgium

[4]Canberra – Bumn Areva, Meriden, USA

The availability of Application Specific Integrated Circuits (ASICs) for the readout of radiation detectors represents a valuable resource for the development of compact, low-power detection systems and/or systems with multiple readout channels. A limitation often encountered in the development of ASICs for radiation detectors, and somehow intrinsic to their scope (and to the acronym as well), is their specificity to a given detector application, which makes the re-use of the same ASIC for different detectors quite problematic if not impossible.

In this work we present the circuit VERDI-3 (Versatile Readout for Detector Integration -3), an integrated circuit developed to provide a unique readout solution for different families of radiation detectors, from nitrogen-cooled Ge and Si(Li) detectors, to silicon drift detectors (SDDs), to scintillation detectors, to photomultipliers tubes and others. The detectors can have an output capacitance from 0.1pF to 39pF, while the energy range spreads from 300eV to 3MeV with both signal polarities, positive and negative. The readout scheme can be pulsed-reset or continuous-reset with an optional external zero-network. All the configurations have been studied to get good noise performance.

The new VERDI chip is characterized by a revised programmable shaping amplifier and baseline holder, a new embedded biasing network and a revised SPI communication with added functions.

The circuit includes 8 channels, each one composed by a hybrid charge preamplifier, a shaping amplifier, a baseline holder, a peak stretcher and an output power buffer. An on-chip selector provides at the output of each channel the waveform of a specific stage, including an RC integrator for external digital processing of the signal. Alternatively, the 8 channels may be multiplexed on a single output for low-speed, low-power random readout. Different settings, like gain, shaping time, preamplifier compensation and many others can be externally programmed by SPI for the specific detector to be readout. The VERDI chip can operate in “gamma” or “x ray” mode, according to the application, matching the several usage modalities of radiation detectors. Only the input JFET, feedback capacitor and reset device are left external to the ASIC, to be chosen specifically for each detector as shown fin Fig.1.

In the work, we will present the experimental results obtained with different kinds of detectors, like Ge, Si(Li), SDD and SSDD detectors, demonstrating the versatility of the VERDI chip.

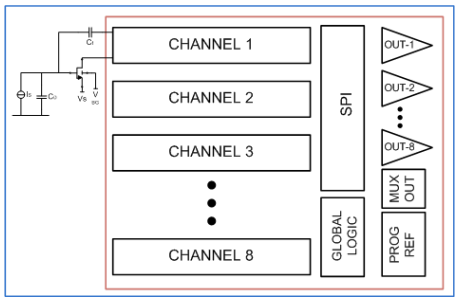

Fig. 1 – Readout scheme. Inside the red box the general architecture of the ASIC

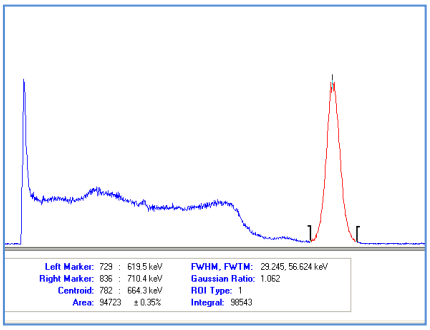

Fig. 2 – A ^{137}Cs spectrum of a 3 cm2 SSDD-scintillator coupled with 2 channels of the 8 channels VERDI ASIC. A resolution of 4.3%@1µsec shaping time (2.4 µsec peaking time) at 662 keV is reached at 20 °C