ULTRA-FAST COMPACT MULTI-CHANNEL READOUT SYSTEM FOR SDDs

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Several X-ray spectroscopy applications (e.g. at synchrotron facilities) requires detection systems operating with high-energy resolution and high-counting rate capability. The use of Silicon Drift Detectors (SDDs) is very often the best option to cope with such demanding requirements. Even with SDDs, the segmentation of the detector in separate units allow to further increase the overall count-rate capability by subdividing the photon flux in more independent units. In this framework, the use of ASICs (Application Specific Integrated Circuits) for the readout of multi-elements SDDs allows to handle the number of channels within a very compact architecture of the detection system with low power consumption and maintaining excellent noise performance.

This paper describes a complete read-out system specifically designed for speed and compactness demanding multi-channel applications, based on SDDs. The system is composed of a Front-End ASIC (layout shown in Fig. 1) and of a compact PCB Acquisition System (Fast-DAQ) for data acquisition and ASIC programming. Software for spectra visualization and ASIC control completes the system.

The ASIC is hosted on a PCB board providing all bias and filtering. It performs contemporary read-out of 8 independent Silicon Drift Detectors, providing a 8:1 multiplexed analog output (fast mode) or two separate 4:1 multiplexed analog outputs (ultra-fast mode). Each one of the 8 analog channels includes a charge sensitive preamplifier (with a rise time of 30ns) operating in the pulsed-reset regime, a 9-complex-pole shaper, a baseline holder, fast peak stretcher and an efficient pile-up rejection system exploiting a fast shaping amplifier. The circuit is completely programmable by the Fast-DAQ: the user can choose 3 different shaping times (270ns, 680ns, and 1.8us), 4 gain settings, independent threshold level for each channel, or completely kills the unused channels. The ASIC is able to autonomously generate the reset signal for the detector or receive and synchronize the detector reset from the DAQ; the pulse width of such reset can be adjusted as well according to the detector needs. During the reset of the SDDs, the ASIC internally inhibits the analog part in order to have the minimum dead time possible. The biasing current and the voltage reference for all the ASIC stages is internally generated and can be adjusted from the DAQ, so that no manual trimmering is needed on the boards. A very efficient pile-up-rejector (PUR) has been implemented in order to reject effectively pile-up events but in a less conservative way than in conventional PURs in order to maximize the throughput of good events.

The Fast-DAQ is based on a FPGA and performs both data acquisition and ASIC programming by SPI. It is able to read-out the ASIC Multiplexer up to 10MHz. The data are transmitted from the ASIC board to the Fast-DAQ in differential mode in order to reduce pick-up disturbs. The estimated throughput is 90% when the detector system is operated at 100kcps per channel (Fig. 2). The noise added by the circuit at 1.8µs shaping time is 2.2 electrons. Exploiting the speed capability of the system, the user can read 400kcps flux photons with a 60% throughput, the circuit noise being just 4.1 electrons (270ns shaping time).

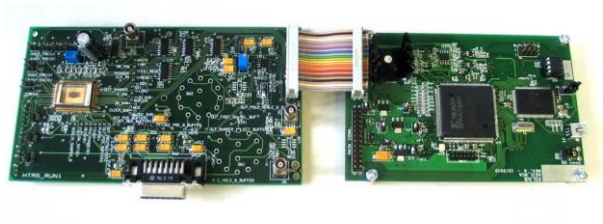

Figure 1 Picture of the complete fast system for multi-channel applications based on SDDs. The left board hosts the 8-channel ASIC, the right board is the fast-DAQ

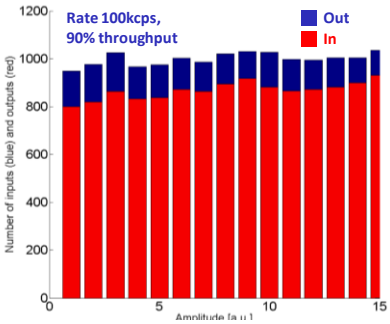

Figure 2 Simulation of 15 thousands events at the input of the detection system at 100kcps rate per channel. The events are distributed uniformly in the output dynamic range. The throughput is 90%.